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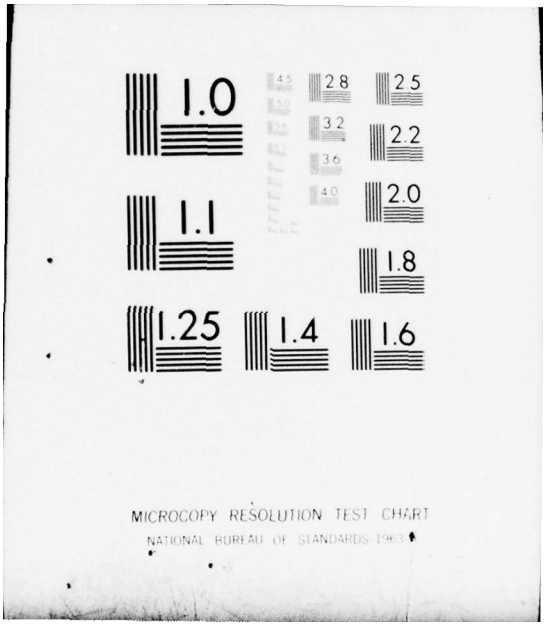
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Research and Development Technical Report
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RESEARCH AND DEVELOPMENT TECHNICAL REPORT
ECOM 75-1329-2

ELECTRON BEAM SEMICONDUCTOR L-BAND AMPLIFIER

B. W. Bell
Watkins-Johnson Company
3333 Hillview Avenue
Palo Alto, CA 94304

July 1976

Second Triannual Report for Period 1 September through 31 December 1975

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(18) (19) **REPORT DOCUMENTATION PAGE**		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER ECOM-75-1329-2	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER (9)
4. TITLE *(and Subtitle)* (6) Electron Beam Semiconductor L-Band Amplifier		5. TYPE OF REPORT & PERIOD COVERED 2nd Triannual rpt. no. 2 1 Sept 1975 – 31 Dec 1975
		6. PERFORMING ORG. REPORT NUMBER (14) W-J – 22-4142R2
7. AUTHOR(s) (10) Bruce W. Bell		8. CONTRACT OR GRANT NUMBER(s) (15) DAAB07-75-C-1329
9. PERFORMING ORGANIZATION NAME AND ADDRESS Watkins-Johnson Company 3333 Hillview Avenue Palo Alto, CA 94304		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS (16) 1S7 62705 AH 94 B3 11
11. CONTROLLING OFFICE NAME AND ADDRESS		12. REPORT DATE July 1977 (17) B3 13. NUMBER OF PAGES 26
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)* US Army Electronics Command Fort Monmouth, NJ 07703 ATTN: DRSEL-TL-BS		15. SECURITY CLASS. *(of this report)* Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited. (11) Jul 76

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

(12) 31p.

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Electron Beam Semiconductor
EBS diode
output matching circuit
diode processing

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The goal of this program is to develop a 2000 watt L-Band amplifier capable of operating at a 1 percent duty cycle with 25 dB gain and an operating lifetime of 10,000 hours. During this period, two EBS diode runs were processed, the target holder, output matching circuit, and output RF window were designed, and four exploratory models were fabricated, evaluated and tested.

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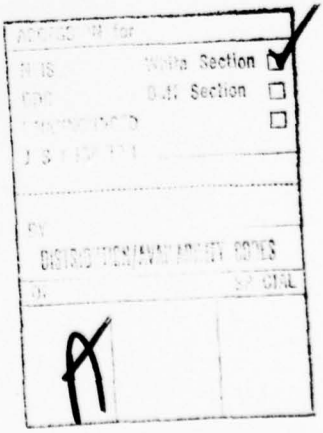


LIST OF ILLUSTRATIONS

1. INTRODUCTION

a. Objective

The objective of this program is the development of a 2000 W EBS L-band amplifier capable of operating at a 1 percent duty cycle with 25 dB gain and with an operating lifetime of 10,000 hours. The EBS amplifier will be designed with the goal of a unit cost less than $100 when produced in quantities of 10,000. Two of the units will be life tested for 1000 hours during the course of the program and three units will be delivered at the end of the program to USAECOM for further evaluation and test.

b. Technical Approach

The device used to meet these goals will be a grid-controlled EBS amplifier with an externally mounted matching network. The basic configuration of the amplifier is shown in Fig. 1-1. The essential elements of this device are the electron gun, semiconductor target, and matching network. The electron gun produces a circular electron beam which is density modulated by an RF signal applied to the grid. The electron beam strikes the semiconductor target producing large current gain by impact ionization. To develop the large amount of power required, the diode is matched into a low impedance, typically about three ohms. The matching network then impedance transforms the diode source impedance into 50 ohms. The same design has been used on the WJ-3620, an EBS amplifier that developed over 700 W of peak power at 950 MHz.

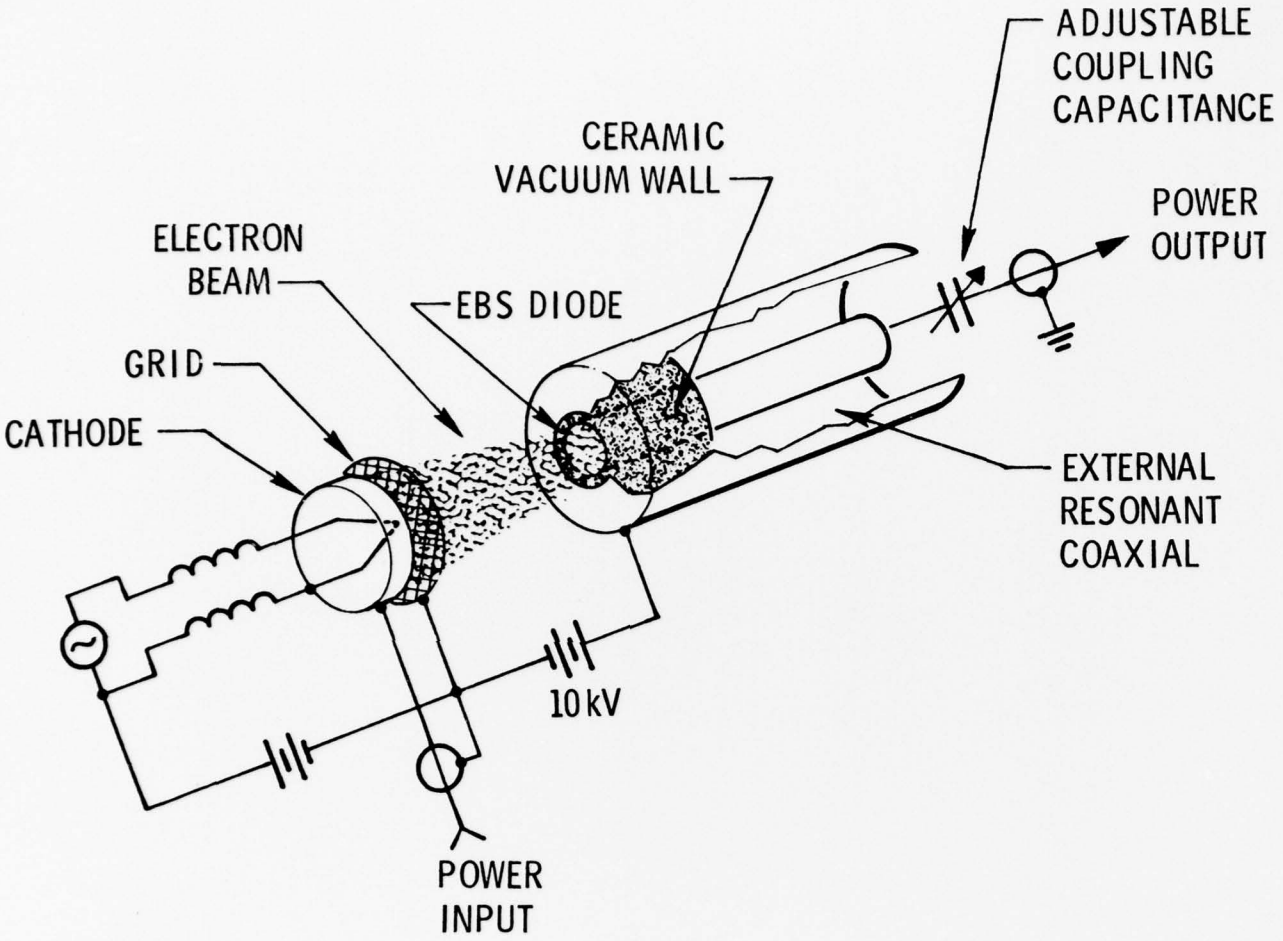


FIG. 1-1 - Schematic of EBS L-Band Amplifier

2. PROGRAM SUMMARY

a. Summary of Work

During the second tri-annual reporting period the design of the output matching circuit, target holder, and output window was completed. Modifications were made to the optics of the original gun assembly of the WJ-3620 to produce the required diameter electron beam. Parts were ordered and assemblies were fabricated and cold-tested.

The diode mask set was completed and two diode runs were fabricated. The diode breakdown voltages varied from 250 to 300 volts and were within 10 percent of the predicted breakdown voltages. The excess capacitance factor was less than 1.2 for the diodes, considerably better than previous devices.

Four amplifiers were assembled during this reporting period. WJ-3620 S/N 3 demonstrated up to 570 W peak output power. Oscillation problems which damaged the diode in S/N 2 were eliminated by shielding of the input circuitry from the output. Heater open circuits on S/N 4 and S/N 5 prevented testing of these units; modifications made to the heater and heater leads have remedied this problem.

b. Program Schedule

Figure 2-1 shows the program plan. Shading of the bars indicates the tasks which have been completed since the beginning of the program. The program plan is current as of 12/31/75.

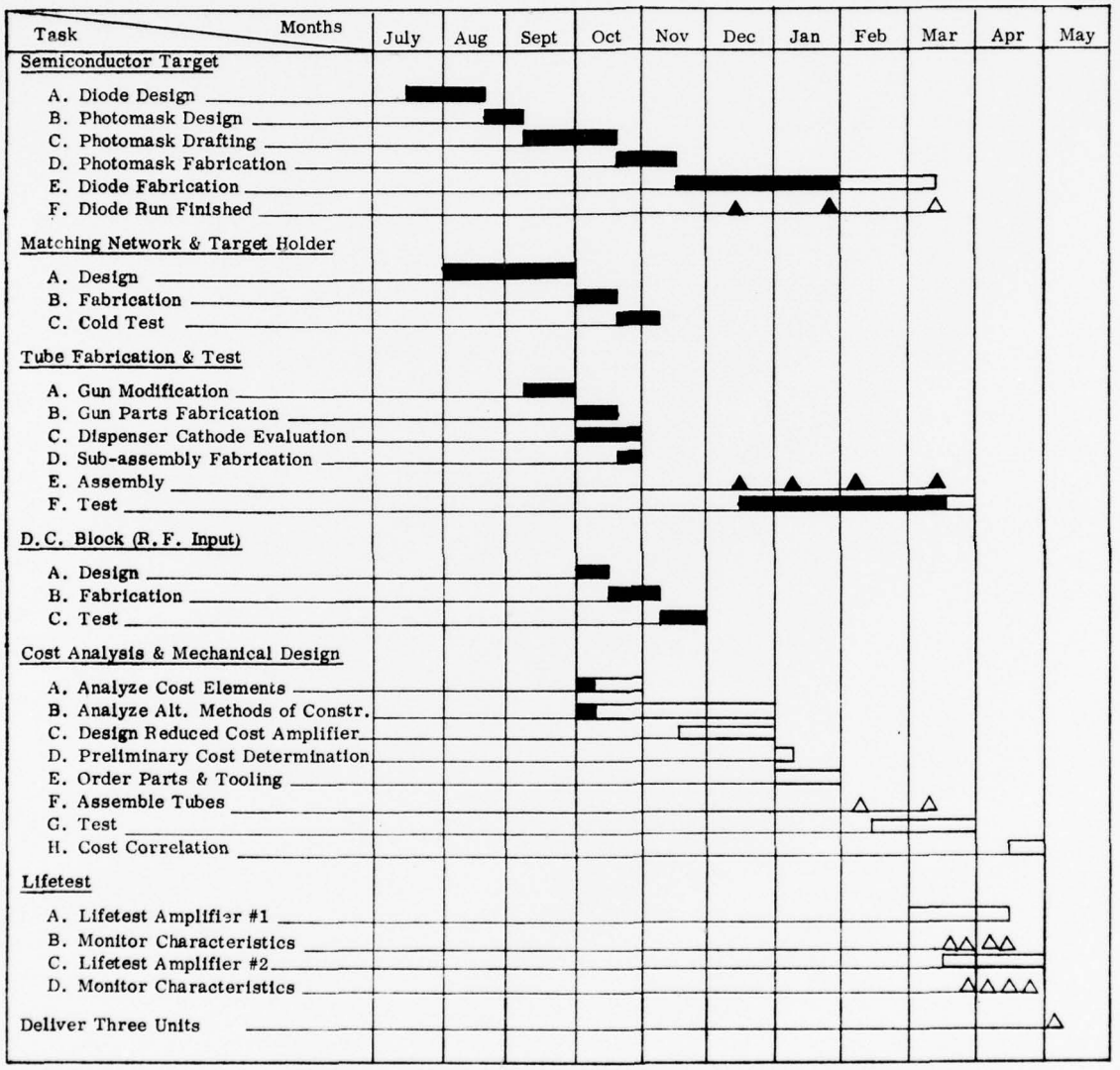


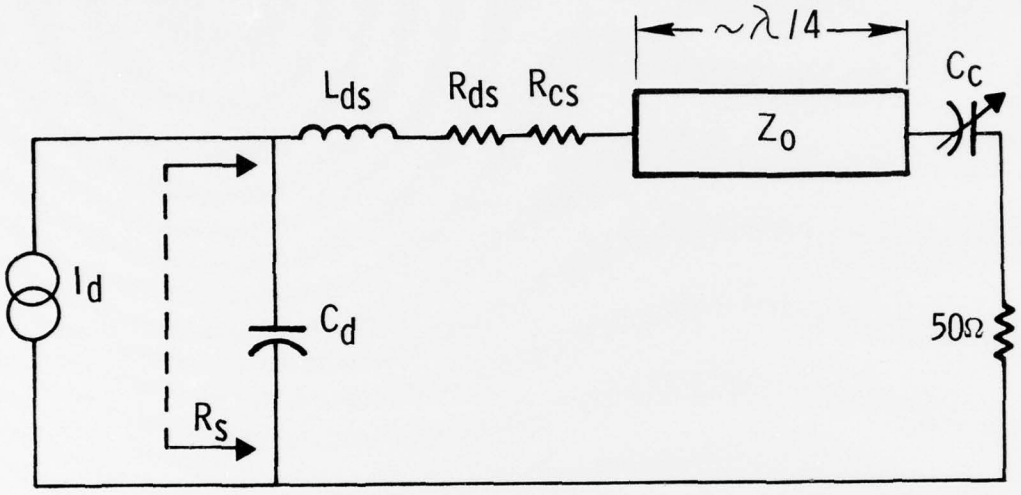
Fig. 2-1. Program Plan

3. OUTPUT MATCHING CIRCUIT

The output matching circuit is used to match the diode into the low source impedance required to generate the high peak output powers and then transform this source impedance up to the 50 ohm output impedance. The matching circuit consists of a quarter-wave cavity in series with a variable capacitor. Fig. 3-1 shows a schematic of the circuit and the diode . By varying the capacitance, it is possible to vary the source impedance. R_{cs} represents the resistive losses through the cavity and at the finger contact joining the cavity to the output window. It is important to minimize these resistive losses, because at the low output impedances at which the device is operated, any losses seriously degrade the target efficiency.

A photograph of the completed cavity is shown in Fig. 3-2. At the low impedance (near) end of the cavity, a large diameter BeCu finger contact is used to connect the center conductor of the cavity to the center conductor of the output window. The large area of contact is designed to minimize the RF losses. At the 50 ohm end of the cavity, an OSM connector is used which connects to the center conductor of the cavity by another BeCu finger contact. To adjust the coupling capacitance, a metal sleeve slides over a gap in the center conductor; by adjusting the position of this sleeve the capacitance can be varied.

The cavity was measured with a network analyzer to determine the resonant frequency and Q of the cavity. A short was used in place of the output window and target holder, so that only the losses of the cavity would be measured. Under these conditions, the resonant frequency was 1005 MHz and the Q was 1150, representing a resistive loss of .017 ohms. With the addition of the coax-line for biasing of the diode, the Q was reduced to 600, or a total cavity resistive loss of .033 ohms. The low losses show that the BeCu finger contacts are providing a very good RF contact.



Where:

I_d:	Diode Output Current
R_s:	Diode Source Impedance
C_d:	Diode Shunt Capacitance
L_{ds}:	Diode and Target Inductance
R_{ds}:	Diode and Target Series Resistance
R_{cs}:	Cavity Series Resistance
Z_o:	Characteristic Cavity Impedance
C_c:	Adjustable Coupling Capacitance

Figure 2. Schematic of Diode Plus Output Matching Circuitry

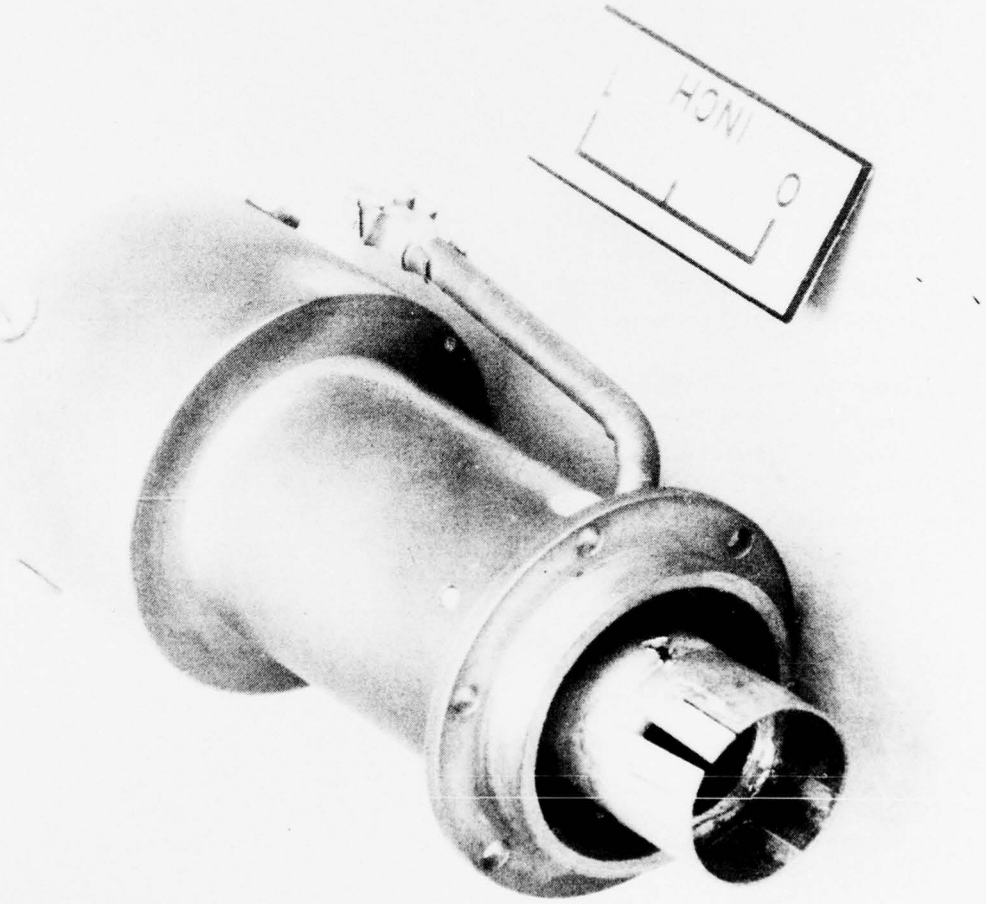


Fig. 3-2 - Photograph of the output cavity.

4. TARGET HOLDER AND OUTPUT WINDOW

The target holder and output window assembly provides a mechanical mounting for the diode and beam mask, heat sinking for the diode, and provides the window for coupling the RF through the vacuum wall. As in the design of the cavity, it is important to minimize the RF losses; in addition, the thermal impedance from the diode to the heat sink should be maintained as low as possible. Three different output window designs were evaluated to determine which gave the best combination of low thermal impedance and low RF losses. All three designs utilize a BeO ceramic to provide the electrical isolation between the center and outer conductor and to provide the low thermal impedance. The first design, window #1, utilizes a flat BeO ceramic disc to provide a compromise between thermal and RF losses. Window #2 provides a very good thermal path with a larger volume of ceramic, which increases the RF losses. Window #3 utilizes a very low volume of ceramic to minimize RF losses at the sacrifice of some thermal impedance.

To compare the designs, the RF losses were measured with the network analyzer. Wire bonds were used to form a short circuit in place of the EBS diode, to eliminate the effect of any losses of the diode. Window #1 was measured first; 109 1.5 mil aluminum wires were used to form the short-circuit. The measured Q was 400 at a center frequency of 975 MHz. The total resistive loss of window #1 is .049 ohms; since this includes the .033 ohm loss of the cavity, the RF loss of .016 ohms through the window and wire bonds is quite low. It was also possible to measure the effect of the number of wire bonds on performance, to determine how many wire bonds are needed on a target. Wires were gradually removed while the effect on the Q and center frequency were measured. Table 4-I summarizes the results. Above 50 wires, there is almost no additional effect on performance. The shift in center frequency is caused by the increased inductance of the target as the number of wire bonds is reduced. The inductance of a single wire bond, calculated from this shift in frequency, is 1.62 nH, which is within five percent of the theoretical inductance for a length of wire of the given diameter.

The second window was measured under the same conditions. The measured Q was 300 at a center frequency of 887 MHz. The lower center frequency is a result of the larger volume of ceramic in the window. The resistive loss in the window and wire bonds was double that of the first window, .032 ohms. However, even these losses are quite low; because of this, it was decided not to test the third window, as both of the first two designs offer lower thermal impedances with excellent RF performance.

TABLE 4-I

EFFECT OF THE NUMBER OF WIRE BONDS
ON UNLOADED Q AND CENTER FREQUENCY

No. of Wire Bonds	Unloaded Q	Center Frequency
1	85	728
2	118	850
4	188	919
6	209	936
8	219	941
10	239	948
12	254	952
15	284	959
20	327	967
25	346	965
32	369	968
42	390	970
52	397	972
62	394	974
75	398	975
90	398	975
109	402	975

5. DC BLOCK

A DC block was fabricated for the RF input to allow introduction of the RF signal at ground potential instead of floating the supply at the cathode potential of 10 kV. The DC block was designed to stand off a minimum of 15 kV while minimizing the insertion loss. A photograph of the completed design is shown in Fig. 5.1. Hi-potting of the completed design showed that it would stand off 15 kV, although for reliable operation the voltage should not be allowed to exceed 14 kV. The performance of the device was measured on the network analyzer; Fig. 5-2 shows a plot of loss versus frequency. The DC block has a very wide bandwidth; the -1 dB bandwidth extends from 325 MHz to 1600 MHz.

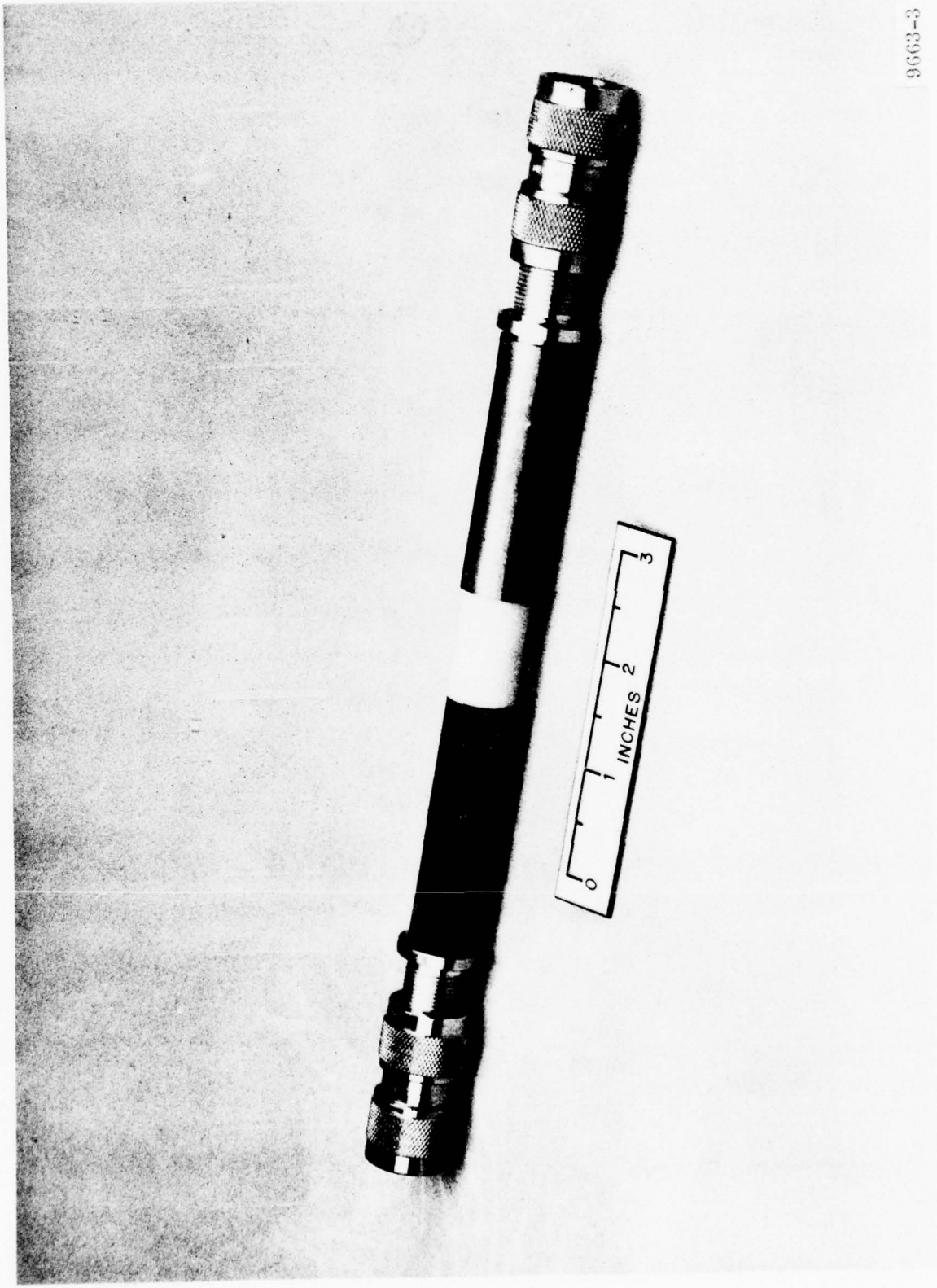


Fig. 5-1 - Photograph of the DC Block

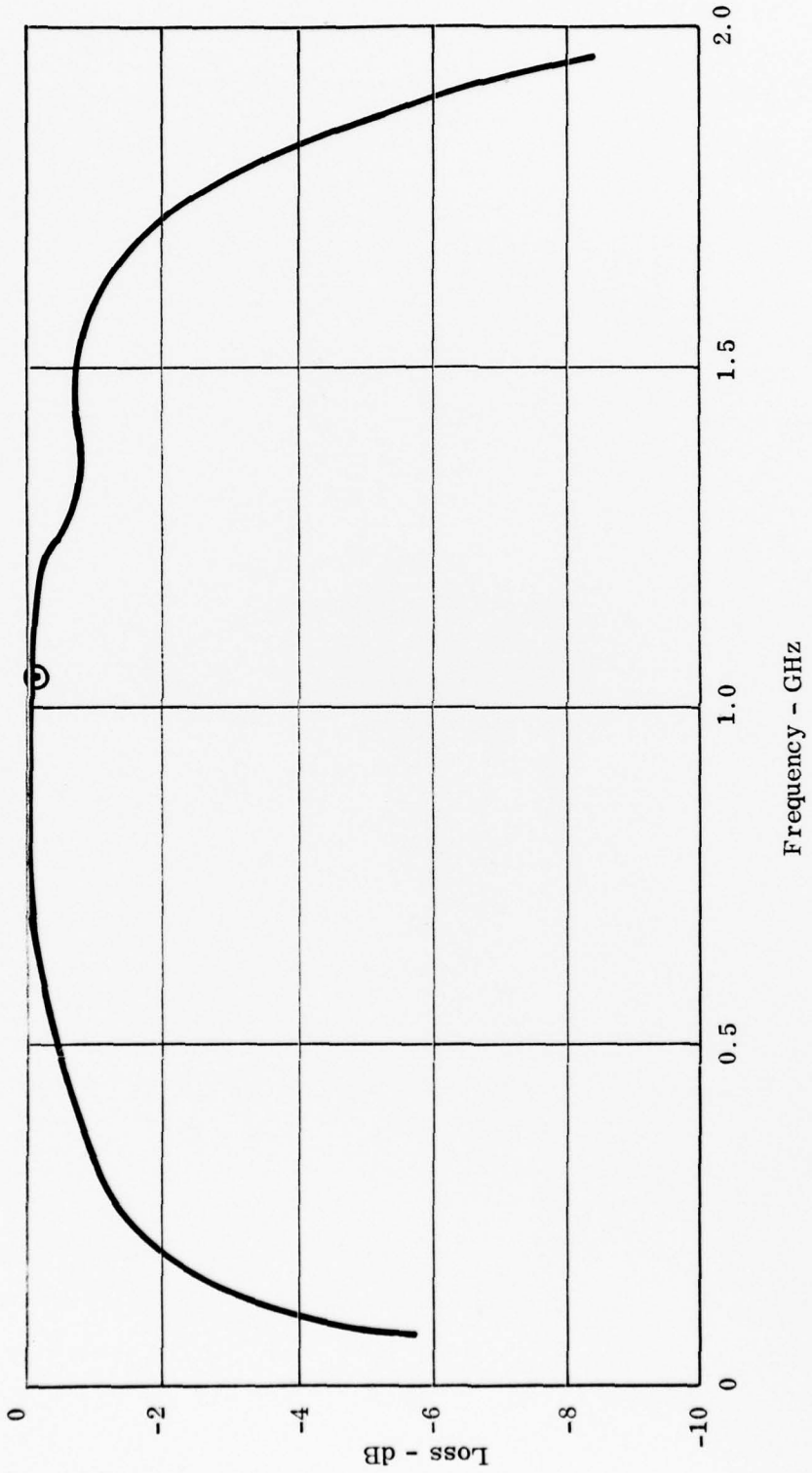


Fig. 5-2 - Measured loss of DC block versus frequency.

6. DIODE PROCESSING RESULTS

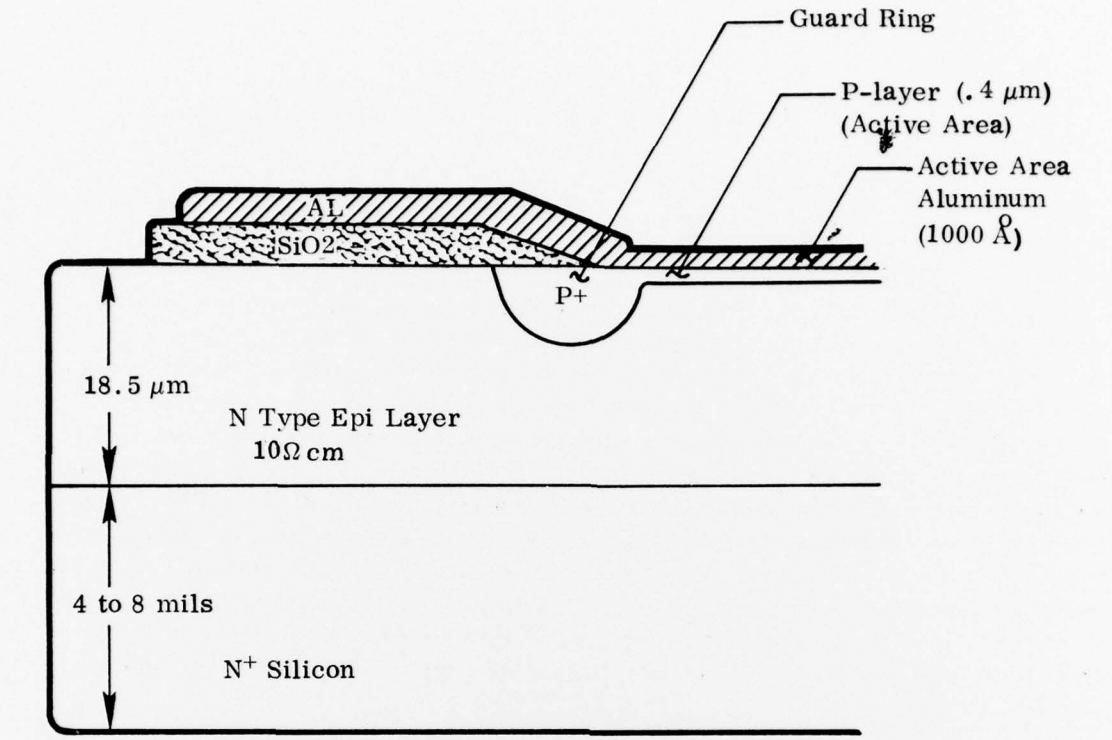
Fabrication of the new diode mask set was completed during this second tri-annual period and two diode runs were fabricated. The diodes have an active area of 12.3 mm^2 with a circular geometry; there are 42 diodes on each wafer. Fabrication of these diodes is similar to that of other EBS diodes, although the area is larger than most other types of EBS diodes, which reduces the yield that can be expected. As discussed in the first tri-annual report, the diodes can be fabricated using one of two techniques to control the breakdown voltage. These are summarized in Fig. 6-1. The first technique uses a guard-ring to control the diode breakdown voltage. For a given material thickness and doping, there is an optimum guard ring depth to maximize the diode breakdown voltage. The second technique uses a metal field plate over the diode junction to control the diode breakdown voltage in addition to the use of the guard-ring. This technique will result in diodes with higher breakdown voltages than with just the guard-ring; however, the use of the field plate increases the diode capacitance. To evaluate the difference in breakdown voltage and capacitance, diodes have been fabricated using both of these techniques.

a. Diode Run #1

Five wafers were processed in the first diode run. Table 6-I lists the characteristics of the wafers used in this run and the processing involved. The mask set 101 is the 12.3 mm^2 mask set designed for this program; the 761 mask set is a 2.5 mm^2 rectangular diode geometry mask set which was used as a control. The Epi thickness varied from 17 to 25 μm prior to processing; during processing, the high doping concentration in the N+ region diffuses into the epitaxial region, reducing the thickness of the epi. The typical reduction in Epi thickness is 3 to 4 μm.

The processing results are listed in Table 6-II. As expected, the capacitance of the diodes with the field plates was higher than those without by 10 percent. However, in both cases, the excess capacitance factor is very low, ranging from 1.1 to 1.2. The design goal for these diodes was an excess capacitance factor of 1.5, while the best ever achieved with EBS diodes previously had been 1.3. The very low excess capacitance factor of these diodes can be attributed to the large active area to perimeter area ratio of these diodes, since the excess capacitance results primarily from the perimeter area.

The leakage currents measured for these diodes was greater than that of most previous EBS diode runs produced here at Watkins-Johnson; the typical leakage current values at breakdown were 1 to 5 mA. It is suspected that the higher leakage current values were introduced during the masking step to open up the active area of the



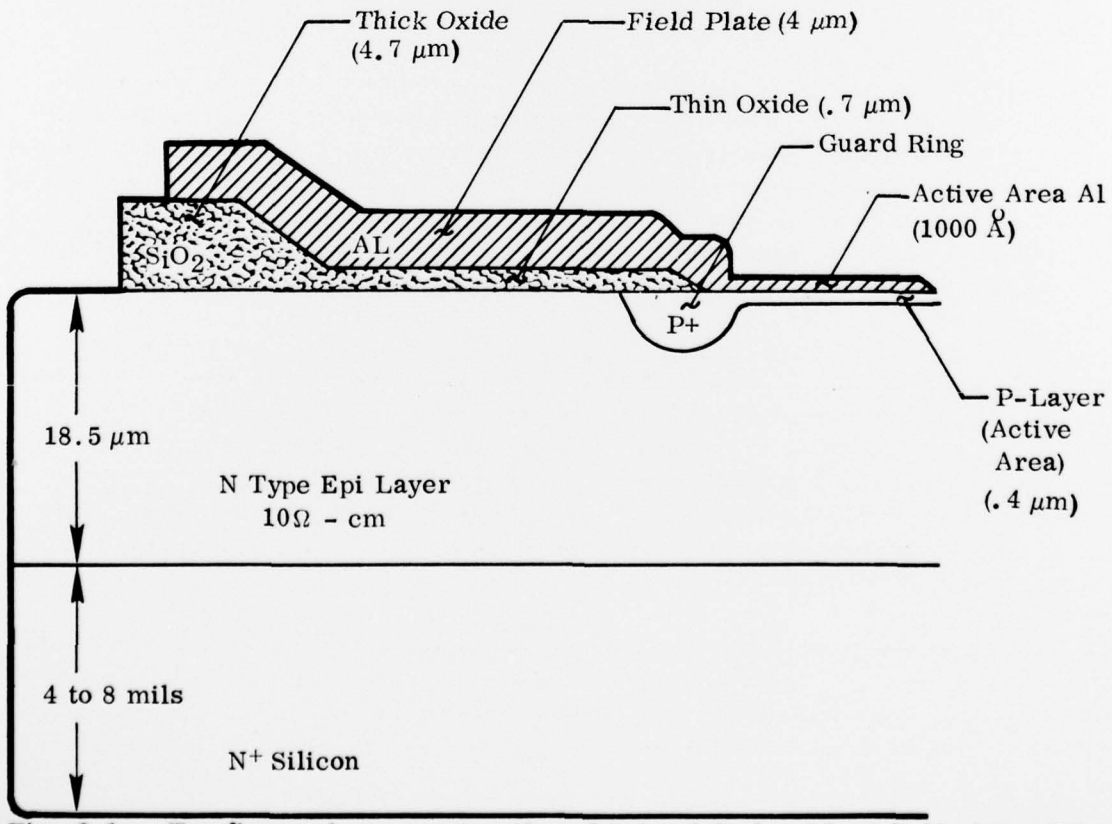


Fig. 6-1a - Top figure shows construction of L-band diode without field plate. Note that most of the thick aluminum is separate from the diode by a thick oxide layer.
Fig. 6-1b - Bottom figure shows construction of L-band diode with field plate.

TABLE 6-I

DIODE RUN #1 - WAFER CHARACTERISTICS

Wafer	Epi	Doping	Mask Set	Field Plate
1	22 μm	12 ohm-cm	101	yes
2	22 μm	12 ohm-cm	101	no
3	22 μm	12 ohm-cm	761	yes
4	25 μm	9.8 ohm-cm	101	yes
5	17 μm	10 ohm-cm	101	yes

TABLE 6-II

DIODE RUN #1 - WAFER RESULTS

Wafer	Breakdown Voltage	Leakage Current	Capacitance	Excess Capacitance Factor
1	250-280 V	.5 - 5 mA	92 pF @ 100 V	1.2
2	230-250 V	.5 - 5 mA	84 pF @ 100 V	1.1
3	180-220 V	1 - 5 mA	17.5 pF @ 100 V	1.15
4	230-245 V	1 - 5 mA	76 pF @ 100 V	1.2
5	No yield; caused by defective material			

EBS diodes. During processing, prior to the definition of the active area of the diode a layer of thermal oxide is grown on top of the epitaxial layer. This oxide is removed over the active area and the layer is diffused into the epi layer. However, during processing, the oxide was not completely removed, but rather islands of oxide were left, which prevented proper diffusion of the p-layer. This was discovered during subsequent probing of the wafers which showed low breakdown voltages for all of the diodes. The active area was remasked to completely remove the oxide and the p-layer was diffused in again, which resulted in a p-layer which is twice as deep as it should be in most places and the proper depth in the areas where the oxide originally was. This reprocessing resulted in diodes with the expected breakdown voltages, as shown in Table 6-II; however, due to the concentration of the electric field at the points where the oxide originally was, the leakage current at these points is also increased. To avoid a re-occurence of the problem, the diode processing has been modified for future runs to perform the active area diffusion prior to growing of the oxide layer.

b. Diode Run #2

Processing of a second diode run was begun to fabricate diodes with lower leakage currents than the diodes in the first run. Table 6-III lists the characteristics of the wafers used in this run. The table also lists the resulting breakdown voltages and yields. The diodes from this run had good yields; in addition, the diodes showed lower leakage currents; typically the leakage current at 200 V was less than .5 mA.

c. Diode Fabrication Yield

The average yield per wafer of the first two diode runs varied from 10 to 40 percent, which is considerably lower than yields on smaller diodes processed at the Watkins-Johnson diode laboratory. A diode run was processed using the 101 mask set but with extremely pure bulk silicon material. The material was 2000 ohm-cm bulk material; two wafers were processed. The result was the fabrication of diodes with greater than 1000 V breakdown with 90 percent yield. The result of this test is that the yield loss is being introduced primarily by the defect density of the Epi-material in conjunction with the larger diode area. In comparison, the expected yield for semiconductor devices with an equivalent area is only 10 percent, indicating that the yields are very satisfactory.

TABLE 6-III

DIODE RUN #2 - WAFER CHARACTERISTICS AND RESULTS

Wafer	Epi Thickness	Resistivity	Voltage	Yield
1	21.8 μm	12 ohm-cm	250-280 V	38%
2	21.8 μm	12 ohm-cm	230-280 V	43%
3	21.8 μm	12 ohm-cm	235-285 V	17%
4	25.2 μm	9.8 ohm-cm	170-260 V	33%
5	18 μm	11 ohm-cm	-	-

7. AMPLIFIER FABRICATION AND TEST RESULTS

The L-band amplifier is composed of three basic sub-assemblies; the heater-cathode assembly, the body assembly, and the target assembly. The target assembly is fabricated by brazing the diode down to the copper center conductor, typically with Au-Ge preform which has a melting point of 357° C. The diode is then wirebonded in place and checked electrically. Finally, the beam mask is located over the diode. Fig. 7-2 shows a photograph of the target assembly after the diode has been wirebonded in place.

After the tube is assembled, it is baked out overnight at 300° C. The dispenser cathode is activated while the unit is at temperature. The device is then cooled down and pinched off from the main vacuum pump; a 2 l/s pump is used to pull the final vacuum. The device is burned in for several days to stabilize the cathode. The circuitry is connected to the device and it is ready for test.

During assembly of the first device, it was found that after brazing of the diode down to the copper center conductor, the diode surface would begin to ripple, indicating that there was internal stress developed by the mismatch in thermal expansion between the copper and the silicon diode. A moly pellet was made to act as an interface layer between the copper and the silicon. Although the moly increases the thermal impedance, the thermal expansion closely matches the silicon. Several test assemblies were made and heat-cycled. None showed any signs of ripple on the diode surface.

a. WJ-3620 S/N 2

The first device assembled for this program used a diode from the first run, wafer #2. The diode was brazed down to a 40 mil thick moly pellet which, in turn, was brazed down to the copper center conductor. The output window was #1, with the flat BeO ceramic. The grid-cathode spacing was set at 12 mils cold, about 10 mils hot. The device was set up on the network analyzer to measure the center frequency and the total resistive losses with the diode in place. With the diode biased at 100 V, the center frequency was 970 MHz and the unloaded Q was 166, which is equivalent to a resistive loss of .111 ohms. This value of resistive loss is what was originally calculated for the design; Fig. 3-5 of the first tri-annual report (ECOM-75-1329-1) shows the expected circuit efficiency with this value of loss.

The device was set up on test under low duty cycle operation. It was noticed while monitoring the cathode current that an oscillation was present in the pulse, even at low peak output powers of 10 W. When the input power was increased, the diode supply crowbar fired and the diode was found to be damaged. Apparently the oscillation became severe enough to sustain the pulse when the input was turned off, causing

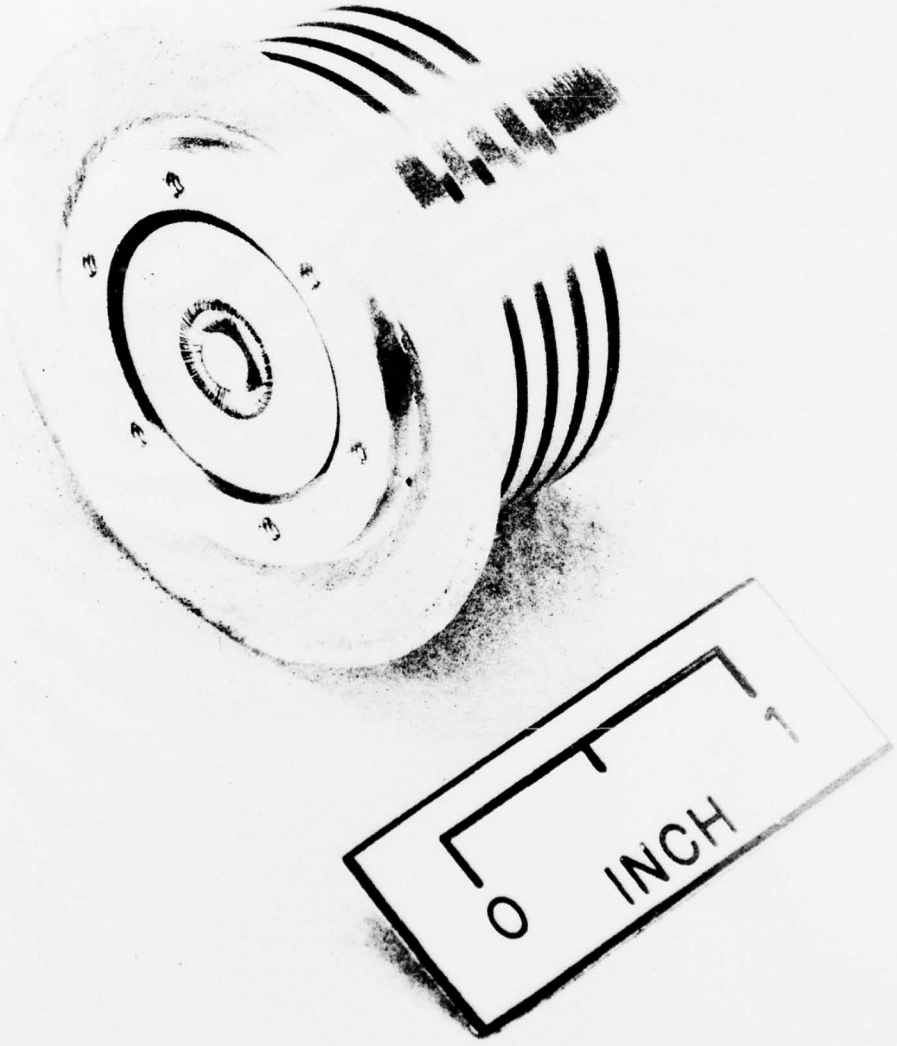


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Fig. 7-1 - Photograph of target assembly with diode brazed in place and wirebonded. The screw holes are provided for attachment of the beam mask assembly.

the diode to exceed the duty cycle rating. Because of the large capacitor used to hold up the pulse voltage (75 μF), the diode supply crowbar was not able to prevent the diode from damage.

b. WJ-3620 S/N 3

S/N 3 was built using a new diode from the first run, wafer #2; the target, gun, and heater-cathode assemblies were re-used from S/N 2. Fig. 7-2 shows a photograph of the diode I-V characteristics after the tube was assembled, prior to bakeout and testing. To prevent a re-occurrence of the oscillation that damaged the diode in S/N 2, shielding was installed between the input and output circuitries of the device. The cathode current was carefully monitored for any oscillation; however, none was present. The device was tested at peak output powers up to 570 W at .1 percent duty, and a frequency of 970 MHz. Table 7-I lists the maximum peak output powers achieved as the bias voltage was increased. Fig. 7-3 shows a graph of the transfer curve measured at a diode bias voltage of 90 V and a beam voltage of 11 kV. While operating under these conditions, the diode was damaged; the cause of failure was not established, but it is suspected that the failure occurred at a point defect location where the high current density caused a punch through to occur in the silicon.

The target efficiency measured for S/N 3 was typically 35 percent, which was lower than expected. The cause of this was the relatively large grid-cathode spacing, which introduced a transit-time loss to the beam. At a 10 mil spacing, the transit-time efficiency would be 60%. To increase this efficiency to 90 percent, the grid-cathode spacing would have to be decreased to 5 mils. This modification is quite straight-forward, requiring additional shims under the body assembly prior to brazing of the body and heater-cathode assemblies together. The modification will be made on the next tube to be assembled.

c. WJ-3620 S/N 4, 5

S/N 4 was built with another diode from the first run, wafer #2. However, during bakeout of this unit, the heater open-circuited, which was caused by the relatively high heater current of 3A. To remedy this, a new heater-cathode assembly was used on S/N 5 which required only 1.7 A versus the 3A of the earlier design. In addition, the grid to cathode spacing was moved in to a 7 mil hot spacing, to improve the transit-time efficiency through the grid-cathode region. When the tube was set up on test, the heater in this unit also open-circuited at even the lower current level. Examination of the failed assembly showed that the nickel heater leg, which is spot-

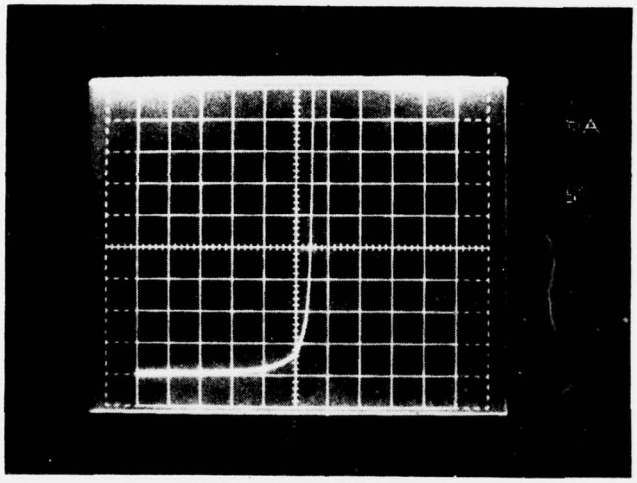

Fig. 7-2 - I=V characteristic of diode in S/N 3 after assembly of tube completed.

TABLE 7-I

WJ-3620 S/N 3 - PERFORMANCE CHARACTERISTICS

Bias Voltage	P_{in}	P_{out}
30 V	30 dBm	22 W
40 V	30 dBm	67 W (26% target efficiency)
50 V	35 dBm	157 W
60 V	35 dBm	217 W
70 V	36 dBm	362 W
80 V	36 dBm	491 W
90 V	36 dBm	570 W (36% target efficiency)

welded to the tungsten-rhenium heater, was melting at the spot-weld. Hence, the diameter of the nickel lead was increased from 10 to 20 mils to reduce the current density in the nickel lead. The modification was evaluated on test assemblies and found to be capable of handling currents in excess of 3A.

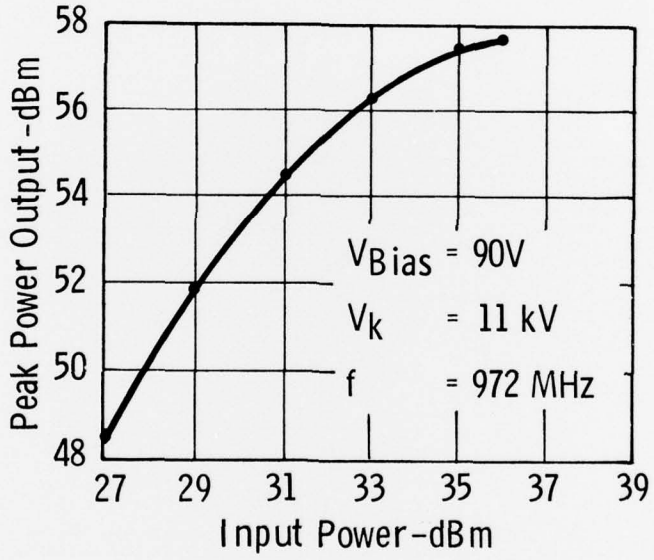

Figure 5. Transfer Curve for EBS Amplifier WJ-3620 S/N 3

8. PROGRAM FOR THE NEXT INTERVAL

During the next reporting period the following tasks are schedule for completion:

1. Evaluate the effect of decreasing the cathode-grid spacing on device efficiency.
2. Test diodes from the second diode run, in order to achieve higher output power levels.
3. Begin life test of two amplifiers.